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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/606,860	06/28/2000	David W. Carr	14004100253	7037

25697 7590 10/17/2005

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EXAMINER	
PHAN, MAN U	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/606,860	CARR, DAVID W.	
	Examiner	Art Unit	
	Man Phan	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,13-19,21-26 and 28* is/are rejected.

7)☒ Claim(s) *3,10-12,20 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The application of Carr for a "Method and apparatus for packet reassembly in a communication switch" filed 06/28/2000 has been examined. Claims 1-28 are pending in the application.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "210" has been used to designate both Reassembly Circuitry (as shown in Fig. 2) and routing circuitry as described in the specification page 5, line 25.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference character (580) described in page 11, line 13 for Fig. 3.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4-8 and 18-19, 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aramizu et al. (US#6,493,356) in view of Ganmukhi et al. (US#6,233,243).

With respect to claims 18-19 and 21-25, both Aramizu (US#6,493,356) and Ganmukhi (US#6,2333,243) disclose a novel system for performing reassembling packets in an ATM communication network according to the essential features of the claims. Aramizu discloses a segmentation and reassembly system cooperating with a data processing system having at least one central processing unit connected through a CPU interface and special purpose engines, and the segmentation and reassembly system comprises a plurality of frame buffers for storing pieces of data selectively supplied from first ATM cells and a processing means connected to the plurality of frame buffers for selectively accessing the pieces of data and selectively supplying at least selected pieces of data to the special purpose engines through an exclusive interface for modifying the pieces of data, thereby improving the throughput of the segmentation and reassembly system (Col. 2, lines 8 plus). Aramizu further teaches in Fig. 1 a block diagram illustrated the segmentation and reassembly system comprising the composite processing units 51, 52, . . . , 5j and 5k, an internal bus system 6 connected between the frame buffers 31 to 3n and the composite processing units 51 to 5k, a buffer memory 7 connected to the composite processing unit 51, a CPU interface controller 8 for a CPU interface and a controller 9. Though

not shown in FIG. 1, the composite processing units 51 to 5k are accompanied with a memory, a data buffer or latch circuits. The memory, a data buffer or the latch circuits may be incorporated in the composite processing units 51 to 5k. The composite processing units 51 to 5k are connected to the engines 111 to 11k through interfaces 201/202/ . . . /20j/20k, respectively. A composite processing unit 51/52/ . . . /5j/5k may access pieces of composite data stored in the frame buffers 31/32/ . . . /3n 1/3n, and communicates with the associated engine 111/112/ . . . /11k through the interface 201/202/ . . . 20j/20k. Plural composite processing units 51/52/ . . . /5j/5k can sequentially or concurrently access pieces of composite data stored in one of the frame buffers 31 to 3n under the arbitration of the controller 9, and independently communicate with the associated engines 111 to 11k through the interfaces 201 to 20k. The composite processing units 51 to 5k achieve the following tasks. The different tasks may be assigned to the composite processing units 51 to 5k (Col. 3; lines 8 plus).

However, Aramizu does not expressly disclose the step of when a subsequent cell of the packet is determined to be an end of message cell indicating the end of the packet, completing reassembly of the packet in the buffer to produce a reassembled packet, queuing the reassembled packet for transmission to a destination and deallocating the reassembly context. In the same field of endeavor, Ganmukhi et al. discloses a method and apparatus for performing virtual circuit merging in the egress port of a network switch which minimizes inherent delays in store and forward VC merging techniques and additionally provides the ability to utilize smaller reassembly cell buffers. Ganmukhi teaches in Fig. 2 a block diagram illustrated an egress portion of an I/O module, in which cells received at the output port 16 are stored within the appropriate cell buffer 40 associated with the CID for the respective cell. If the CID is one of a

plurality of CIDs having a common group ID (GID), the GID identifier is also stored in association with the cell buffer within the buffer memory 41. A first flag (F) is also stored in association with the cell buffer which indicates whether or not a complete packet has been received and stored within the respective cell buffer. An End of Packet (EOP) Detector 44 monitors incoming cells and signals Cut through control logic 46 when an EOP is detected. The control logic 46 causes the F flag to then be set for the corresponding CID thus indicating that a complete packet has been received. More specifically, if transmission of a packet has not been commenced via cut through as hereinafter discussed and an EOP condition is detected by the EOP detector 44, the F flag is set via the cut through control logic to indicate that a complete packet has been stored within the respective cell buffer 40. The cut through control logic 46 is also coupled to a transmit scheduler 48 which schedules completely assembled packets for transmission over the respective egress communications link 18 (See Fig. 3 and Col. 4, lines 30 plus).

Regarding claims 1-2 and 4-8, they are method claims corresponding to the apparatus claims 18-19 and 21-25 above. Therefore, claims 1-2 and 4-8 are analyzed and rejected as previously discussed with respect to claims 18-19 and 21-25.

One skilled in the art would have recognized the need for effectively and efficiently reassembling packets using a limited number of reassembly context in an ATM communication network, and would have applied Ganukhi's novel use of the performing VC merging in the egress port of a network switch into Aramizu's reassembling packet system cooperating with a data processing and special purpose engines for achieving a high throughput. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was

made to apply Ganmukhi's method and apparatus for performing cut-through virtual circuit merging into Aramizu's segmentation and reassembly system for ATM communication network improved in throughput with the motivation being to provide a method and system for reassembling packets using a limited number of reassembly contexts.

6. Claims 9, 13-17 and 26, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aramizu et al. (US#6,493,356) in view of Ganmukhi et al. (US#6,233,243) as applied to the claims above, and further in view of O'Neill et al. (US#6,243,382).

With respect to claims 9, 13-17 and 26, 28, Aramizu and Ganmukhi disclose the claimed limitations discussed in paragraph 5 above. However, Aramizu and Ganmukhi do not expressly disclose the claimed feature of the traffic management block for receiving indication that packets corresponding to reassembly contexts of the plurality of reassembly contexts are ready for transmission. In the same field of endeavor, O'Neill et al. discloses a switching apparatus, for use in an ATM network, includes a switch fabric for switching ATM cells, a segmentation and reassembly device for reassembling packets from ATM cells, and a plurality of traffic management devices. Each traffic management device receives ATM cells delivered to associated ports of the apparatus and is connected by a first data delivery path to the switch fabric and by a second data delivery path directly to the segmentation and reassembly device. The traffic management device identifies those received ATM cells that belong to one or more predetermined types of packets, requiring reassembly by the segmentation and reassembly device, as respective reassembly cells. The traffic management device then delivers received cells other than such identified reassembly cells to the switch fabric via its first data delivery path

for switching by the switch fabric, and then delivers the reassembly cells to the SAR device via the second data delivery path for reassembly into packets. The reassembly cells do not pass through the switching fabric in the course of transfer from the traffic management device to the segmentation and reassembly device (See Fig. 2; Col. 8; lines 36 plus).

One skilled in the art would have recognized the need for effectively and efficiently reassembling packets using a limited number of reassembly context in an ATM communication network, and would have applied O'Neill's traffic management device for use in an ATM switching and Ganmukhi's novel use of the performing VC merging in the egress port of a network switch into Aramizu's reassembling packet system cooperating with a data processing and special purpose engines for achieving a high throughput. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply O'Neill's interfacing to SAR devices in ATM switching apparatus and Ganmukhi's method and apparatus for performing cut-through virtual circuit merging into Aramizu's segmentation and reassembly system for ATM communication network improved in throughput with the motivation being to provide a method and system for reassembling packets using a limited number of reassembly contexts.

Allowable Subject Matter

7. Claims 3, 20 and 10-12, 27 are objected to as being dependent upon the rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

8. The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest wherein storing each of the subsequent cells in the buffer further comprises appending each of the subsequent cells to the linked list, wherein updating the reassembly context further comprises updating the tail pointer of the linked list to reflect addition of each of the subsequent cells to the linked list, as recited in claims 3 and 20; wherein the egress circuit is included in a communications switch that includes a plurality of ingress circuits and a switching fabric, wherein the source is an ingress connection provided to one of the ingress circuit, wherein the routing circuitry receives cells corresponding to a plurality of ingress connections provided to at least a portion of the plurality of ingress circuits, wherein the routing circuitry allocates and deallocates reassembly context to packets received via the plurality of ingress connections, and wherein the routing circuitry perform cyclical redundancy check verification for packet received, wherein when cyclical redundancy check verification indicates that an at least partially received packet has been corrupted, the routing circuitry may cause the at least partially received packet to be purged, as recited in claims 10 and 27.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Takiyasu et al. (US#5,113,392) is cited to show the communication apparatus for reassembling packets received from network into message.

The Hebb et al. (US#6,463,067) is cited to show the submission and response architecture for route loop up and packet classification requests.

The Opalka et al. (US#6,259,699) is cited to show the system architecture for and method of processing packets and/or cells in a common switch.

The Logsdon (US#5,862,355) is cited to show the method and apparatus for overriding bus prioritization scheme.

The Galand et al. (US#5,956,341) is cited to show the method and system for optimizing data transmission line bandwidth occupation in a multipriority data traffic environment.

The Runner (US#6,618,376) is cited to show the ATM utopia bus snooper switch.

The Field et al. (US#6,621,828) is cited to show the fused switch core and method for a telecommunications node.

The Chung et al. (US#6,487,203) is cited to show the apparatus for transmitting cells between ATM layer and physical layer and method therefor

The Norton et al. (US#5,898,688) is cited to show the ATM switch with integrated system bus

The Ferguson et al. (US#5,809,024) is cited to show the memory architecture for a local area network module in an ATM switch

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149. The examiner can normally be reached on Mon - Fri from 6:00 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at toll free 1-866-217-9197.

Mphan

10/07/2005.

MAN U. PHAN
PRIMARY EXAMINER